AA-64 architecture segment registers

CS, SS, DS, ES, FS, GS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	internal descriptor cache		
CS for a segment or a selector																32bit base	32bit limit	access rights
SS for a segment or a selector																32bit base	32bit limit	access rights
DS for a segment or a selector																32bit base	32bit limit	access rights
ES for a segment or a selector																32bit base	32bit limit	access rights
FS for a segment or a selector																64bit base #1	32bit limit	access rights
GS for a segment or a selector																64bit base #1	32bit limit	access rights

note	description
#1	The upper 32 bits can be set to non-zero values through MSRs.