AA-64 architecture initial state

initial processor state after RESET and INIT		
register	after RESET	after INIT
RAX	0000_0000_0000_0000h or BIST result	0000_0000_0000_0000h or BIST result
RBX	0000_0000_0000_0000h	0000_0000_0000_0000h
RCX	0000_0000_0000_0000h	0000_0000_0000_0000h
RDX	0000_0000_0000_TFMSh (see CPUID)	0000_0000_0000_TFMSh (see CPUID)
RSP	0000_0000_0000_0000h	0000_0000_0000_0000h
RBP	0000_0000_0000_0000h	0000_0000_0000_0000h
RSI	0000_0000_0000_0000h	0000_0000_0000_0000h
RDI	0000_0000_0000_0000h	0000_0000_0000_0000h
R8	0000_0000_0000_0000h	0000_0000_0000_0000h
R9	0000_0000_0000_0000h	0000_0000_0000_0000h
R10	0000_0000_0000_0000h	0000_0000_0000_0000h
R11	0000_0000_0000_0000h	0000_0000_0000_0000h
R12	0000_0000_0000_0000h	0000_0000_0000_0000h
R13	0000_0000_0000_0000h	0000_0000_0000_0000h
R14	0000_0000_0000_0000h	0000_0000_0000_0000h
R15	0000_0000_0000_0000h	0000_0000_0000_0000h
RIP	0000_0000_0000_0000h	0000_0000_0000_0000h
RFLAGS	0000_0000_0000_0002h	0000_0000_0000_0002h
CS	selector=F000h base=FFFF_0000h limit=0000_FFFFh access rights=0093h, writeable	selector=F000h base=FFFF_0000h limit=0000_FFFFh access rights=0093h, writeable
SS	selector=0000h base=0000_0000h limit=0000_FFFFh access rights=0093h	selector=0000h base=0000_0000h limit=0000_FFFFh access rights=0093h
DS	selector=0000h base=0000_0000h limit=0000_FFFFh access rights=0093h	selector=0000h base=0000_0000h limit=0000_FFFFh access rights=0093h
ES	selector=0000h base=0000_0000h limit=0000_FFFFh access rights=0093h	selector=0000h base=0000_0000h limit=0000_FFFFh access rights=0093h
FS	selector=0000h base=0000_0000_0000_0000h limit=0000_FFFFh access rights=0093h	selector=0000h base=0000_0000_0000_0000h limit=0000_FFFFh access rights=0093h
GS	selector=0000h base=0000_0000_0000_0000h limit=0000_FFFFh access rights=0093h	selector=0000h base=0000_0000_0000_0000h limit=0000_FFFFh access rights=0093h
GDTR	base=0000_0000_0000_0000h limit=0000_FFFFh (access rights=0082h)	base=0000_0000_0000_0000h limit=0000_FFFFh (access rights=0082h)
IDTR	base=0000_0000_0000_0000h limit=0000_FFFFh (access rights=0082h)	base=0000_0000_0000_0000h limit=0000_FFFFh (access rights=0082h)
LDTR	selector=0000h base=0000_0000_0000_0000h limit=0000_FFFFh access rights=0082h	selector=0000h base=0000_0000_0000_0000h limit=0000_FFFFh access rights=0082h
TR	selector=0000h base=0000_0000_0000_0000h	selector=0000h base=0000_0000_0000_0000h

	limit=0000_FFFFh access rights=0082h	limit=0000_FFFFh access rights=0082h
CR0	0000_0000_6000_0010h	0000_0000_x000_0010h [#1]
CR2	0000_0000_0000_0000h	0000_0000_0000_0000h
CR3	0000_0000_0000_0000h	0000_0000_0000_0000h
CR4	0000_0000_0000_0000h	0000_0000_0000_0000h
CR8	0000_0000_0000_0000h	unmodified
DR0	0000_0000_0000_0000h	0000_0000_0000_0000h
DR1	0000_0000_0000_0000h	0000_0000_0000_0000h
DR2	0000_0000_0000_0000h	0000_0000_0000_0000h
DR3	0000_0000_0000_0000h	0000_0000_0000_0000h
DR6	0000_0000_FFFF_0FF0h	0000_0000_FFFF_0FF0h
DR7	0000_0000_0000_0400h	0000_0000_0000_0400h
ST0..ST7	+0.0	unmodified
MM0..MM7	0000_0000_0000_0000h	unmodified
CW	0040h	unmodified
SW	0000h	unmodified
TW	5555h	unmodified
FP_IP64	0000:0000_0000_0000_0000h	unmodified
FP_DP64	0000:0000_0000_0000_0000h	unmodified
FP_OPC	000_0000_0000b	unmodified
XMM0..XMM7	0h	unmodified
XMM8..XMM15	0h	unmodified
MXCSR	0000_1F80h	unmodified
TSC MSR	0000_0000_0000_0000h	unmodified
TSC_AUX MSR	0000_0000h	unmodified
MISC_CTL MSR	PSN enabled	unmodified
MISC_ENABLE MSR	processor-specific	unmodified
EFER MSR	0000_0000h	0000_0000h
SEP_SEL MSR	0000h	unmodified
SEP_RSP MSR	0000_0000_0000_0000h	unmodified
SEP_RIP MSR	0000_0000_0000_0000h	unmodified
STAR MSR	0000_0000_0000_0000h	unmodified
LSTAR MSR	0000_0000_0000_0000h	unmodified
CSTAR MSR	0000_0000_0000_0000h	unmodified
FS_BAS MSR	0000_0000_0000_0000h	0000_0000_0000_0000h
GS_BAS MSR	0000_0000_0000_0000h	0000_0000_0000_0000h
KERNEL_GS_BAS MSR	0000_0000_0000_0000h	0000_0000_0000_0000h
PAT MSR	0007_0406_0007_0406h	unmodified
MTRR_CAP	0000_0000_0000_0508h	unmodified
MTRR_DEF_TYPE	0000_0000_0000_0000h	unmodified
MTRR_PHYS_*	0000_0000_0000_0000h	unmodified
MTRR_FIX_*	undefined	unmodified
MCAR MSR	0000_0000h	unmodified
MCTR MSR	0000_0000h	unmodified
APIC_BASE MSR	FEE0_0x00h (x=9 if BSP, else x=8)	unmodified
TEMP_DR6	0000_0000_0000_0000h	0000_0000_0000_0000h
CAUSING_DB	false	false
SMBASE	0003_0000h	unmodified
IO_RESTART_RIP	0000_0000_0000_0000h	unmodified
IO_RESTART_RCX	0000_0000_0000_0000h	unmodified
IO_RESTART_RSI	0000_0000_0000_0000h	unmodified
IO_RESTART_RDI	0000_0000_0000_0000h	unmodified
IN_REP	false	false
IN_SMM	false	false
IN_HLT	false	false
IN_SHUTDOWN	false	false
IN_FP_FREEZE	false	false

SUPPRESS_INTERRUPTS	false (both bits)	false (both bits)
BLOCK_INIT	false	n/a
BLOCK_SMI	false	false
BLOCK_NMI	false	false
LATCH_INIT	false	n/a
LATCH_SMI	false	false
LATCH_NMI	false	false
A20M#	deasserted high KBC=flat PS/2=pass	unmodified (old) or deasserted high (new) KBC=unmodified PS/2=unmodified (old) or flat (new)
FERR#	deasserted high	unmodified
processor caches	invalidated	unmodified
TLBs, BTB, etc.	invalidated	invalidated
PDPTR0/1/2/3	zero	zero
note	description	
#1	bits 30 (CD) and 29 (NW) remain unmodified