AA-64 architecture processor mode

processor mode								
name	EFER.LMA	CR0.PE	RFLAGS.VM	CS.ar.L	CS.ar.D	CR4.VME	TSS32.IRB [n]	paging?
RM16	0 #1	0	n/a	n/a	0	n/a	n/a	no
RM32					1			
VM16		1	1		0	0	n/a	optional
VM16E0						1	0	
VM16E1							1	
PM16		1	0		0	n/a	n/a	optional
PM32					1			
CM16	1 #2	1	n/a	0	0	n/a	n/a	PAE is required
CM32				0	1			
PM64				1	0			
note	description							
#1	This is known as legacy mode.							
#2	This is known as long mode (LM).							

processor paging								
name	EFER.LMA	CR0.PG	CR4.PAE	CR4.PSE	PDE.PS	page size	table levels	modes
NONE	0	0	n/a	n/a	n/a	n/a	n/a	RM, VM, PM
4K		1	0	0	n/a	4 KB	2	VM or PM
PSE_4K		1	0	1	0	4 KB	2	
PSE_4M					1	4 MB		
PAE_4K		1	1	n/a	0	4 KB	3	
PAE_2M					1	2 MB		
PAE_4K	1	1 #1	1 #1	n/a	0	4 KB	4 #2	CM or PM64
PAE_2M					1	2 MB		
note	description							
#1	The following consistency checks apply:							
#2	The number of table levels depends on the number of implemented virtual address bits. The first implementation supports four levels, to handle 9+9+9+9+12 = 48 virtual address bits. Five or six levels would be required for up to 57 or 64 virtual address bits, respectively.							

bit	transition	check
EFER.LME	from 0 to 1	if (CR0.PG=1) then #GP(0)
	from 1 to 0	
CR0.PG	from 0 to 1	if ((EFER.LME=1) & ((CR4.PAE=0) | (CS.ar.L=1))) then #GP(0)
CR4.PAE	from 1 to 0	if (EFER.LMA=1) then #GP(0)

privilege level			
name	stored in	values	description
IOPL	RFLAGS.IOPL	0..3	I/O privilege level
CPL	SS.CPL or CPL	0..3	current privilege level
RPL	selector.RPL	0..3	requestor privilege level
DPL	descriptor.DPL	0..3	descriptor privilege level

address size

mode		default	67h	effective
Legacy Mode		16	no	16
			yes	32
		32	yes	16
			no	32
Long Mode	CM	16	no	16
			yes	32
		32	yes	16
			no	32
	PM64	64	yes	32
			no	64

operand size

mode		default	66h	REX.W=1	effective
Legacy Mode		16	no	n/a	16
			yes		32
		32	yes		16
			no		32
Long Mode	CM	16	no	n/a	16
			yes		32
		32	yes		16
			no		32
	PM64	32	yes	no	16
			no		32
			ignored	yes	64
		64	yes	no	16
				yes	64
			no	ignored	64
note	The default operand size for PM64 is 32-bit, except for implicit RSP references and near branches. See the one byte opcodes and the two byte opcodes.