

AA-64 architecture

control registers

control registers CR0..15																																
reg.	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW																	reserved								N	E	T	E	M	P		
CR0	reserved																															
	P	C	N	reserved										A	r.	W	reserved								N	E	T	E	M	P		
CR1	reserved																															
	reserved																															
CR2	page fault virtual address																															
	page fault virtual address																															
CR3	reserved												PML4 base #1																			
	PML4 base #1																reserved						P	P	res.							
CR4	reserved																															

	reserved	OS XM EX	OS FX SR	P C E	P G E	M C E	P A E	P S E	D E	T S D	P V I	V M E
CR5	reserved											
	reserved											
CR6	reserved											
	reserved											
CR7	reserved											
	reserved											
CR8	reserved											
	reserved									TPR		
CR9	reserved											
	reserved											
CR10	reserved											
	reserved											
CR11	reserved											
	reserved											

CR12	reserved
	reserved
CR13	reserved
	reserved
CR14	reserved
	reserved
CR15	reserved
	reserved
note	description
#1	The number of actually implemented bits depends on the number of physical address bits. The remaining bits are reserved if less than 52 physical address bits are implemented.

