AA-64 architecture paging

page size and used paging structures									
CR0.PG	CR4.PAE	CR4.PSE	PML2E.PS	page size	CR3 points to	PML4	PML3	PML2	PML1
1	1	x	0	4KB	PML4	512 PML4Es (64bit)	512 PML3Es (64bit)	512 PML2Es (64bit)	512 PML1Es (64bit)
1	1	x	1	2MB	PML4	512 PML4Es (64bit)	512 PML3Es (64bit)	512 PML2Es (64bit)	512 PML1Es (64bit)
note	The number of table levels depends on the number of implemented virtual address bits. The first implementation supports four levels, to handle 9+9+9+9+12 = 48 virtual address bits. Five or six levels would be required for up to 57 or 64 virtual address bits, respectively.								

virtual address translation																					
PS		63		57	56		48	47		39	38		30	29		21	20		12	11	0
4KB		must be canonical (ie. sign-extended)						PML4E #			PML3E #			PML2E #			PML1E #			offset	
2MB		must be canonical (ie. sign-extended)						PML4E #			PML3E #			PML2E #			offset				

2-level 4KB/4MB paging structures																																
entry	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4KB PDE	page table base																				AVL			G	0	D	A	PCD	PWT	U/S	W/R	P
4MB PDE	page base										reserved									PAT	AVL			G	1	D	A	PCD	PWT	U/S	W/R	P
	page base (low)										p.b. (high) [#1]					p. b. (high)																
4KB PTE	page base																				AVL			G	PAT	D	A	PCD	PWT	U/S	W/R	P
note	description																															
#1	The number of actually implemented bits depends on the number of physical address bits. The remaining bits are reserved if less than 41 physical address bits are implemented.																															

3-level 4KB/2MB paging structures																																
entry	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDPTE	reserved												page directory base [#1]																page directory base			
																												P	P			

	page directory base															AVL		res.					CD	WT		res.				P	
4KB PDE	NX	reserved												page table base #1														page table base			
	page table base																					AVL	G	0	D	A	PCD	PWT	U/S	W/R	P	
2MB PDE	NX	reserved												page base #1														page base			
	page base											reserved					PAT	AVL					G	1	D	A	PCD	PWT	U/S	W/R	P	
4KB PTE	NX	reserved												page base #1														page base			
	page base																					AVL	G	PAT	D	A	PCD	PWT	U/S	W/R	P	

note	description
#1	The number of actually implemented bits depends on the number of physical address bits. The remaining bits are reserved if less than 52 physical address bits are implemented.

4-level 4KB/2MB paging structures

entry	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

PML4E	NX	AVL											PML3 base #1																PML3 base			
	PML3 base																					AVL	res.		D	A	PCD	PWT	U/S	W/R	P	
PML3E	NX	AVL											PML2 base #1																PML2 base			
	PML2 base																					AVL	res.		D	A	PCD	PWT	U/S	W/R	P	
4KB PML2E	NX	AVL											PML1 base #1																PML1 base			
	PML1 base																					AVL	G	0	D	A	PCD	PWT	U/S	W/R	P	
2MB PML2E	NX	AVL											page base #1																page base			
	page base											reserved					PAT	AVL					G	1	D	A	PCD	PWT	U/S	W/R	P	
4KB PML1E	NX	AVL											page base #1																page base			
	page base																					AVL	G	PAT	D	A	PCD	PWT	U/S	W/R	P	

note	description
#1	The number of actually implemented bits depends on the number of physical address bits. The remaining bits are reserved if less than 52 physical address bits are implemented.

#PF exception error code

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved											I/D	RSV	U/S	W/R	P